PTOCLM

3/31/05

AS

1. A circuit for use as an active inductor on an integrated circuit having a power supply voltage supplied at a first power supply terminal, comprising:

an metal oxide semiconductor (MOS) transistor having a gate terminal, a drain terminal, and a source terminal, said drain terminal being coupled to said power supply voltage and said source terminal being one of the terminals of said active inductor; and

a resistor having a first terminal coupled to said gate terminal and a second terminal coupled to a voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied at said first power supply terminal and the same sign as said power supply voltage;

said circuit being adapted so that when said circuit is operating said circuit behaves as an active inductor between said source terminal and an other terminal of said active inductor on said integrated circuit.

2. The invention as defined in claim 1 wherein other terminal of said active inductor is said first power supply terminal.

3. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal.

4. The invention as defined in claim 1 wherein MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

5. The invention as defined in claim 1 wherein MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

6. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is higher than a voltage supplied from said second power supply terminal.

7. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is lower than a voltage supplied from said second power supply terminal.

8. The invention as defined in claim 1 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor, said NMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the positive power supply terminal for said integrated circuit and said second power supply terminal is the negative power supply terminal for said integrated circuit.

9. The invention as defined in claim 1 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor, said PMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the negative power supply terminal for said integrated circuit and said second power supply terminal is the positive power supply terminal for said integrated circuit.

10. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage has a larger absolute value than said power supply by one threshold voltage of said MOS transistor.

11. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage is generated from said power supply voltage by a high voltage generator.

12. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

13. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage, said high voltage generator comprising:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a signal that has an average larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator, which said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

14. (Amended) A circuit for use as an active inductor on an integrated circuit, comprising:

a metal oxide semiconductor (MOS) transistor; and

a beyond voltage generator which generates a beyond voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

wherein said MOS transistor is coupled to said beyond voltage generator so as to bias said MOS transistor with said beyond voltage and said MOS transistor is adapted to operate as said active inductor.

15. (Amended) The invention as defined in claim 14 wherein said beyond voltage generator comprises:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a voltage signal that has an average voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that is greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

and a ripple filter which filters said output of said clamp and supplies the output of said beyond voltage generator.

16. (Amended) An integrated circuit comprising a metal oxide semiconductor (MOS) transistor adapted to operate as an active inductor that is biased using a voltage generated on said integrated circuit that is outside the range of the voltage supplied by a power supply off of said integrated circuit for operating said integrated circuit.

17. The invention as defined in claim 16 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

18. The invention as defined in claim 16 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

19. The invention as defined in claim 16 wherein said active inductor is biased by coupling a gate of said MOS transistor to said voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit via an impedance.